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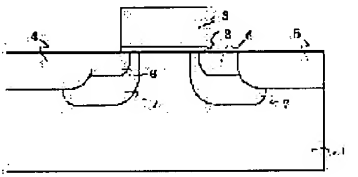
(54) MOS-TYPE SEMICONDUCTOR DEVICE AND ITS PRODUCTION

(57)Abstract:
PURPOSE: To increase the operation speed by improving punch-through breakdown strength, reducing short channel effect and reducing the junction capacitance between a source and a substrate and between a drain and the substrate.
CONSTITUTION: A p+-impurity activating layer 7 to be a punch-through stopper is formed on the bottom side of low-concentration source and drain layers 6 at a part closer to a channel than n-type high concentration impurity activating layers 4 and 5 to be a source and a drain. Since the expansion of the depletion layer in the direction from the source and drain 4 and 5 to the channel is suppressed and the source and drain 4 and 5 are making contact with a substrate 1 without being surrounded by the punch-through stopper 7, the expansion in the direction to the depth of the depletion layer is permitted to be large and the junction capacitance between the source and the substrate and between the drain and the substrate are made small.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to an MOS type semiconductor device and its manufacture method.
[0002]
[Description of the Prior Art] Conventionally, the LDD (Lightly Doped Drain) transistor which has source drain structure as shown in drawing 13 as structure which eases the electric field of the drain section of a short channel transistor is proposed (IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.ED-29, NO.4, 1982).
[0003] The gate electrode 3 is formed through the gate oxide film 2 on the p type semiconductor substrate 1, and, as for this transistor, the impurity active regions 4 and 5 of n type high concentration which serve as a source drain at the right-and-left both sides of this gate electrode 3 are formed, respectively. These n type impurity active regions 4 and 5 are adjoined, and it is n of low concentration [side / channel]. - The impurity active region 6 is formed, respectively.
[0004] Furthermore, in this LDD structure, the DI-LDD (Double Implanted-LDD) transistor which has source drain structure as shown in drawing 14 is proposed as structure of stopping the flare of the depletion layer of the source drains 4 and 5 (VLSI SymposiumTechnical Digest, p42, 1982).
[0005] This DI-LDD structure has the effect which the ion implantation (halo ion implantation) of the impurity of the above-mentioned substrate 1 and this conductivity type is carried out, and p+ type impurity active regions 17 and 17 used as a punch-through stopper were formed, and prevents the punch through between the source drain 4 and 5, and lessens the short channel effects, such as the threshold voltage Vt and sub threshold level swing, and is very effective in short channelization of a transistor so that the source drains 4 and 5 may be surrounded.
[0006]
[Problem(s) to be Solved by the Invention] However, this DI-LDD structure was not able to make [many / not much] the pouring dose of a halo ion implantation.
[0007] That is, in this structure, it is because the junction capacitance between a drain 5 and a substrate 1 will become large between the source 4 and a substrate 1 and a working speed will become slow, if the pouring dose of a halo ion implantation tends to be increased and it is going to make punch-through pressure-proofing high, since the flare of the depletion layer of the source drains 4 and 5 is stopped like ****.
[0008] Although the transistor of the unsymmetrical structure which performed halo pouring only to the source 4 side is also proposed about this point (IEDM Technical Digest, p.617, 1989), if it is in this unsymmetrical structure transistor, it cannot use for the path transistor with which the restrictions on a circuit design increase upwards and which the source 4 and a drain 5 replace.
[0009] The place which this invention is made in order to cancel the above troubles, and is made into the purpose is to offer the LDDMOS transistor which punch-through pressure-proofing of an MOS transistor is made high, and the short channel effects, such as threshold voltage and sub threshold level swing, can be lessened [transistor], and the junction capacitance between the source and a substrate and between a drain and a substrate can moreover be made [transistor] small, and can make a working speed quick, and its manufacture method.
[0010]
[Means for Solving the Problem] In order to attain this purpose, the MOS type semiconductor device concerning this invention The gate insulator layer formed on the semiconductor substrate of one conductivity type, and the gate electrode formed on this gate insulator layer, It is formed in the right-and-left both sides of this gate electrode, and become a source drain field, and also The high concentration impurity active region of a conductivity type, It is formed so that this high concentration impurity active region may be adjoined and it may be located in a channel side. high impurity concentration from the aforementioned high concentration impurity active region The low concentration impurity active region of a conductivity type besides a low, [0011] which is formed in width of face of the same grade as this low concentration impurity active region in contact with this low concentration impurity active-region bottom, is equipped with the impurity active region of one conductivity type with high impurity concentration higher than the aforementioned semiconductor substrate, and is characterized by the bird clapper Moreover, the manufacture method of the MOS type semiconductor device of this invention The process which forms a sidewall in the side attachment wall of the aforementioned gate electrode formed on the semiconductor substrate of one conductivity type, In the process which carries out the ion implantation of the impurity of other conductivity types to the aforementioned

semiconductor substrate by using the aforementioned gate electrode and a sidewall as a mask, and the aforementioned semiconductor substrate top While forming the material used as the mask of an ion implantation in the portion except both the aforementioned gate electrode and a sidewall The process which removes only the aforementioned sidewall alternatively, and the process which carries out the ion implantation of the impurity of other conductivity types to the aforementioned semiconductor substrate by using the aforementioned gate electrode and mask material as a mask, It is characterized by the process which carries out the ion implantation of the impurity of one conductivity type to the aforementioned semiconductor substrate by using the aforementioned gate electrode and mask material as a mask, the process which activates the impurity which added and carried out the ion implantation of the heat treatment, and the thing.

[0012]

[Function] Depletion layer capacitance Cdep between the source and a substrate and between a drain and a substrate It is expressed by the formula 1 when a substrate is a p type semiconductor.

[0013]

[Equation 1] Cdep =rootqepsilonNa/2, Vbi [0014] At the structure where Na is acceptor concentration and the high concentration source drain field was surrounded by the punch-through stopper by halo pouring like DI-LDD structure here, it is Na>Nsub. It becomes. On the other hand, the usual LDD structure without halo pouring is Na=Nsub. Becoming, compared with DI-LDD structure, a depletion layer capacitance becomes small.

[0015] Since the high-concentration source drain field is not surrounded by the punch-through stopper, the LDDMOS transistor of this invention is a formula 1, and it is Na=Nsub. Becoming, a depletion layer capacitance becomes small to the same extent with the usual LDD structure without halo pouring.

[0016] Moreover, what is necessary is just to suppress stretch of the depletion layer from a source drain to the direction of a channel, in order to prevent the punch through between source drains and to lessen threshold voltage and the short channel effect of sub threshold level swing.

[0017] since it comes out from a channel and the punch-through stopper is poured into the bottom of a low concentration source drain field rather than the high concentration source drain field, the LDDMOS transistor of this invention can stop the flare of the depletion layer from a high concentration source drain field and a low concentration source drain field to a channel, can prevent a until punch through to the same extent as a DI-LDDMOS transistor, and can lessen threshold voltage and the short channel effect of sub threshold level swing

[0018]

[Example] Hereafter, the example of this invention is explained based on a drawing.

[0019] The structure of the LDDMOS transistor which is one example concerning this invention is shown in drawing 1 . As for this transistor, high-concentration n type impurity active regions 4 and 5 from which the gate electrode 3 is formed and serves as a source drain field at the right-and-left both sides of this gate electrode 3 are formed through the gate oxide film 2 on the p type semiconductor substrate 1. These n type impurity active regions 4 and 5 are adjoined, and it is n of low concentration [side / channel]. - The type impurity active region 6 is formed, respectively. Moreover, this n - High-concentration p+ with high impurity concentration touch the type impurity active-region 6 bottom, and higher than a substrate 1 The type impurity active region 7 is formed.

[0020] this p+ the type impurity active region 7 -- above-mentioned n- the position where the type impurity active region 6 and a longitudinal direction are the same -- and the depth direction locates and prepares in a deep place -- having -- the width of face -- above-mentioned n- It is set up to the same extent as the type impurity active region 6.

[0021] Next, the drawing 2 - drawing 11 reference is carried out, and the manufacture method of the transistor constituted as mentioned above is explained.

[0022] First, after performing channel pouring for controlling an isolation field and threshold voltage on the semiconductor substrate 1 (not shown), the gate oxide film 2, then the gate electrode 3 are formed (refer to drawing 2).

[0023] Then, further, the silicon-nitride (Si3N4) film 8 used as the stopper of etching is deposited (refer to drawing 3), polycrystal silicon 9' is deposited by CVD (refer to drawing 4), by anisotropic etching, it leaves above-mentioned polycrystal Si film 9' only to the side attachment wall of the gate electrode 3, and sidewalls 9 and 9 are formed after this.

[0024] And-1015cm-arsenic (As) ion of 3 of substrates is poured [1] in by using the gate electrode 3 and the sidewalls 9 and 9 beside [this] a gate electrode (polycrystal Si) as a mask, and, thereby, it is high-concentration n+. Type source drain impurity layer 4' and 5' are formed (refer to drawing 5). Heat treatment is added to these, the activation is performed, and the source drain fields 4 and 5 are formed.

[0025] Then, etchback of the BPSG film 10 is carried out until the gate electrode 3 and sidewalls 9 and 9 are exposed, after depositing and (refer to drawing 6) carrying out a reflow of the BPSG film 10 by CVD (refer to drawing 7).

[0026] Then, the sidewalls 9 and 9 of gate electrode 3 width are removed by the etching method with selectivity, and a window part is formed in a portion with the sidewalls 9 and 9 of gate electrode 3 width (refer to drawing 8).

[0027] The -1014cm-phosphorus (P) ion of 3 is poured in to the window part formed by carrying out etching removal of the sidewalls 9 and 9 of gate electrode 3 width the appropriate back by using the gate electrode 3 and the BPSG films 10 and 10 as a mask, and it is low-concentration n. - Type impurity layer 6' and 6' are formed (refer to drawing 9).

[0028] Then, it is n about the -1013cm-boron (B) ion of 3. - It pours into a field deeper than type impurity layer 6', and p+ impurity layer 7' with concentration higher than a substrate 1 is formed (refer to drawing 10).

[0029] Finally, etching removes 8 the BPSG films 10 and 10 and four layers of Si3Ns, respectively, heat treatment is added, and

it is n. - Type impurity layer 6' and p+ type impurity layer 7' are activated, and it is n. - The type impurity active region 6 and p+ It considers as the type impurity active region 7 (refer to drawing 11).

[0030] Then, the effect of the LDDMOS transistor constituted as mentioned above is explained.

[0031] Drawing 12 shows the potential distribution map in the substrate 1 computed by the device simulation, and is drawing 12 (a). The thing of the usual LDDMOS transistor (structure of drawing 13), and drawing 12 (b) The thing of a DI-LDDMOS transistor (structure of drawing 14) which performed halo pouring, and drawing 12 (c) The thing of the LDDMOS transistor (structure of drawing 1) by this invention is shown, respectively, and the gate length of each transistor is 0.5 micrometers.

[0032] If drain voltage is made high, the depletion layer by the side of a drain will spread to a channel field, it will be connected with the depletion layer by the side of the source, the potential barrier by the side of the source will become low, and a punch through will arise.

[0033] drawing 12 (a) from -- with the usual LDD structure (drawing 13), the depletion layer by the side of a drain is completely connected with the depletion layer by the side of the source, and the punch through has arisen so that clearly

[0034] on the other hand -- drawing 12 (b) And drawing 12 (c) from -- clear -- as -- DI-LDDMOS transistor (drawing 14) With this invention transistor (drawing 1), since the flare to the source and the direction of a channel of the depletion layer of a drain is stopped, the depletion layer by the side of a drain and the depletion layer by the side of the source are completely separated by formation of a punch-through stopper. Therefore, the punch through is prevented in these both.

[0035] On the other hand, the junction capacitance which influences the working speed of equipment is proportional to the inverse number of the source and drain depletion-layer width of face. drawing 12 (a) Drawing 12 (c) from -- clear -- as -- the usual LDDMOS transistor (drawing 13) Since the high concentration source drain field is in contact with the substrate with this invention transistor (drawing 1), the flare to the depth direction of a depletion layer is large. however, drawing 12 (b) from -- it understands -- as -- DI-LDDMOS transistor (drawing 14) **** -- since the high concentration source drain field is in contact with the punch-through stopper field where concentration is higher than a substrate, a depletion layer is short compared with the two aforementioned person

[0036] The above thing shows that the LDDMOS transistor by this invention has the property that few junction capacitances between the source and a substrate and between a drain and a substrate are, highly [punch-through resistance]. Moreover, since there are few flares of the depletion layer to a channel, it also turns out that it has the property that little short channel effect is.

[0037]

[Effect of the Invention] since according to this invention it comes out from a channel and the punch-through stopper is poured into the bottom of a low concentration source drain field rather than the high concentration source drain field as explained in full detail above, the flare of the depletion layer from a high concentration source drain field and a low concentration source drain field to a channel can be stopped, a until punch through can be prevented to the same extent as a DI-LDDMOS transistor, and threshold voltage and the short channel effect of sub threshold level swing can be lessened

[0038] And since a high concentration source drain field was not surrounded by the punch-through stopper but it is in contact with the substrate, the flare to the depth direction of a depletion layer can be large, the junction capacitance between the source and a substrate and between a drain and a substrate can be made small, and, as for the LDDMOS transistor of this invention, the working speed of equipment can be made quick.

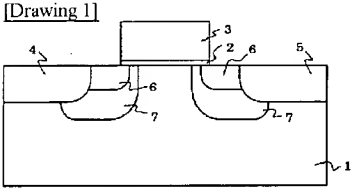
[Translation done.]

* NOTICES *

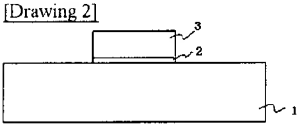
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

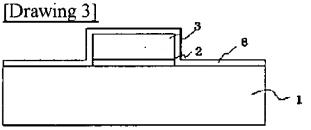
[Drawing 1]



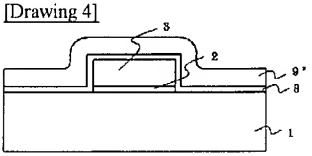
[Drawing 2]



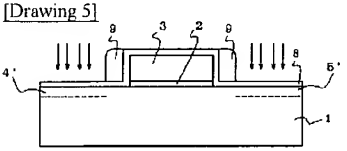
[Drawing 3]



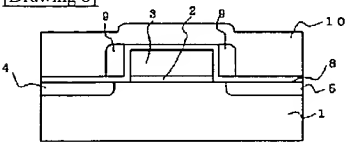
[Drawing 4]



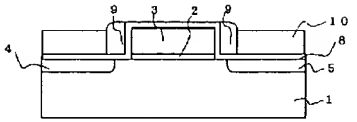
[Drawing 5]



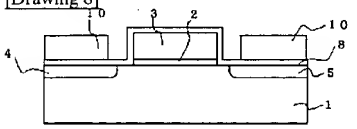
[Drawing 6]



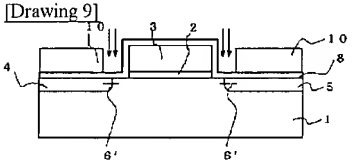
[Drawing 7]



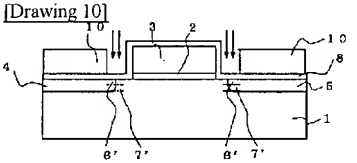
[Drawing 8]



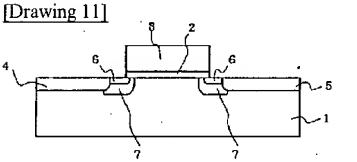
[Drawing 9]



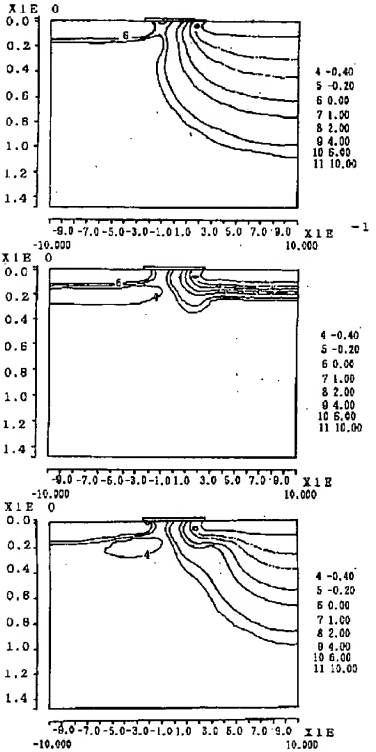
[Drawing 10]



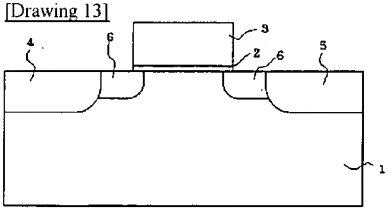
[Drawing 11]



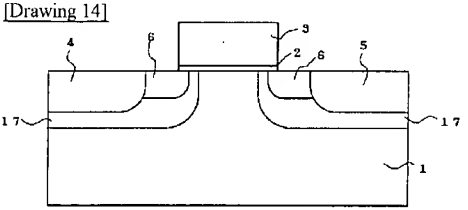
[Drawing 12]



[Drawing 13]



[Drawing 14]



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[Translation done.]

CLAIMS

[Claim(s)]

[Claim 1] The MOS type semiconductor device characterized by providing the following. The gate insulator layer formed on the semiconductor substrate of one conductivity type. The gate electrode formed on this gate insulator layer. It is formed in the right-and-left both sides of this gate electrode, and becomes a source drain field, and also is the high concentration impurity active region of a conductivity type. The impurity active region of one conductivity type with high impurity concentration are formed so that this high concentration impurity active region may be adjoined and it may be located in a channel side, and high impurity concentration is lower than the aforementioned high concentration impurity active region, and also it is formed in width of face of the same grade as this low concentration impurity active region in contact with this low concentration impurity active-region [of a conductivity type], and low concentration impurity active-region bottom, and higher than the aforementioned semiconductor substrate.

[Claim 2] The manufacture method of the MOS type semiconductor device characterized by providing the following. The process which forms a sidewall in the side attachment wall of the aforementioned gate electrode formed on the semiconductor substrate of one conductivity type. The process which carries out the ion implantation of the impurity of other conductivity types to the aforementioned semiconductor substrate by using the aforementioned gate electrode and a sidewall as a mask, While forming the material which serves as a mask of an ion implantation at the portion except both the aforementioned gate electrode and a sidewall in the aforementioned semiconductor substrate top The process which removes only the aforementioned sidewall alternatively, and the process which carries out the ion implantation of the impurity of other conductivity types to the aforementioned semiconductor substrate by using the aforementioned gate electrode and mask material as a mask, The process which carries out the ion implantation of the impurity of one conductivity type to the aforementioned semiconductor substrate by using the aforementioned gate electrode and mask material as a mask, and the process which activates the impurity which added and carried out the ion implantation of the heat treatment.

[Translation done.]